

Fig. 1

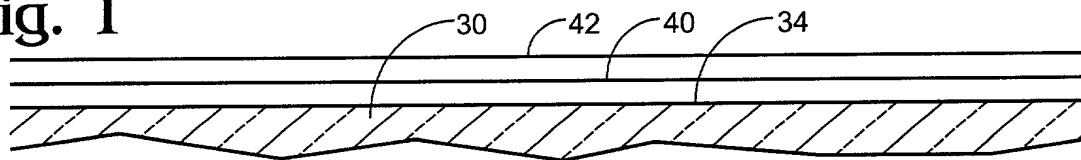


Fig. 2



Fig. 3

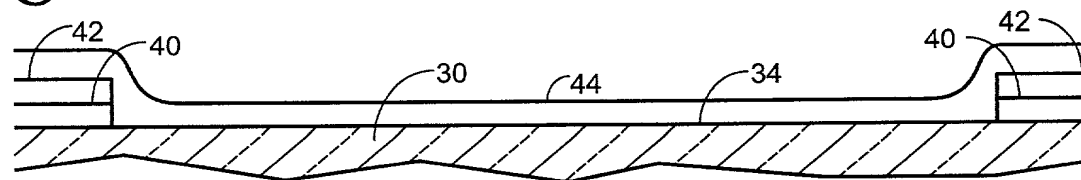


Fig. 4

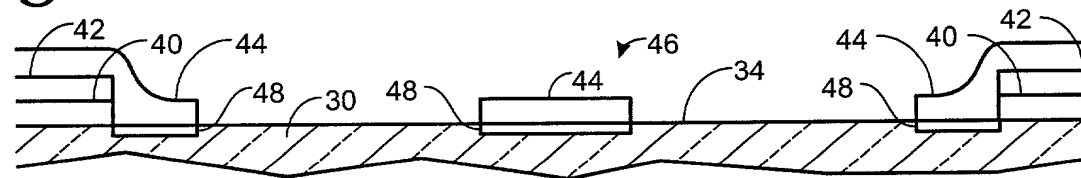


Fig. 5

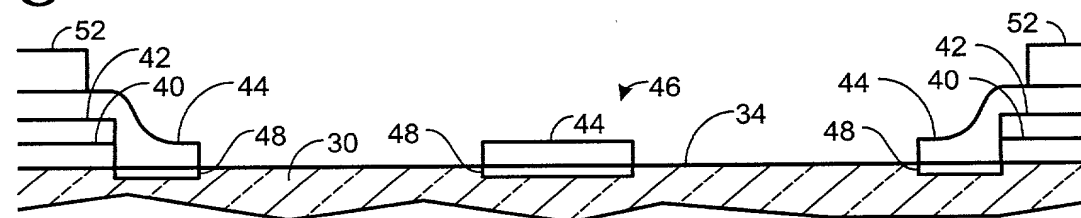


Fig. 6

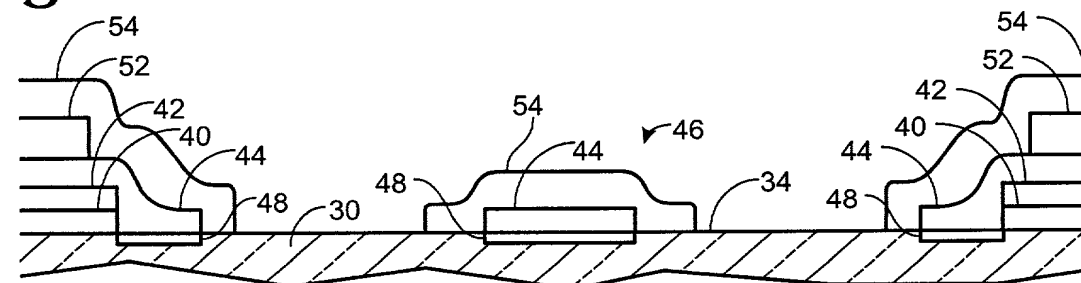


Fig. 7

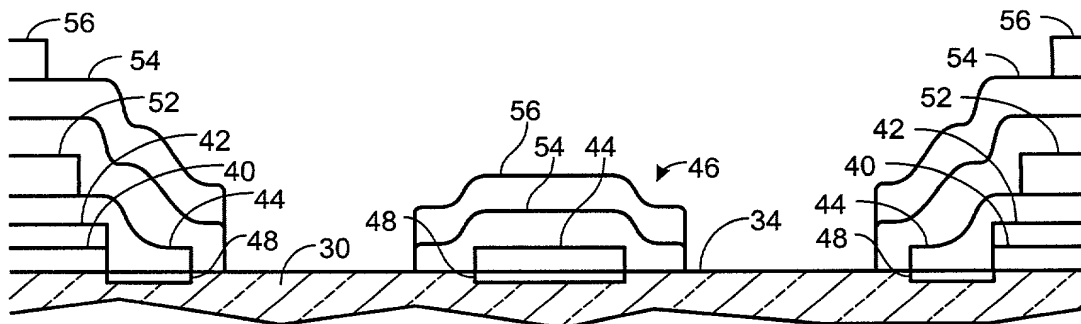


Fig. 9

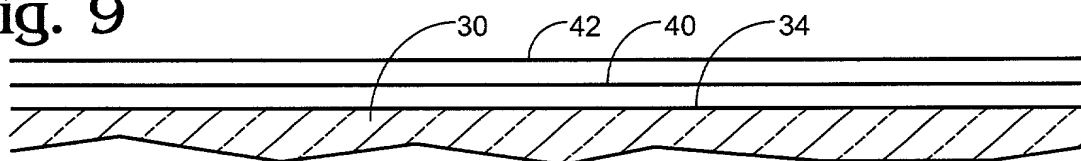


Fig. 10

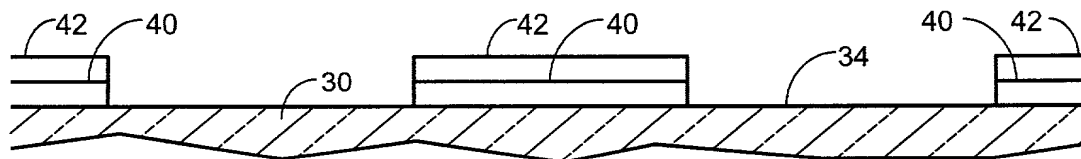


Fig. 11

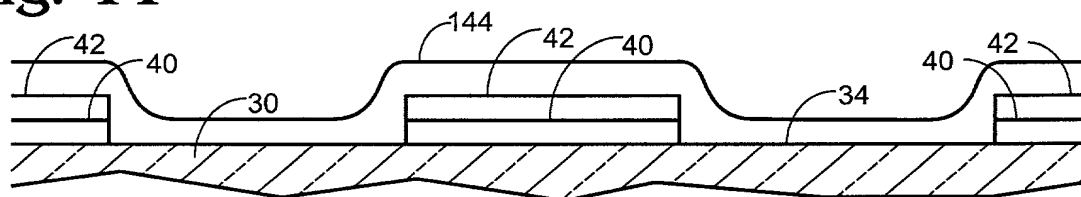


Fig. 12

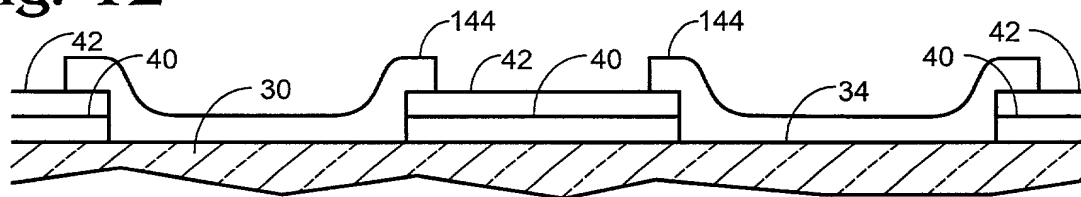
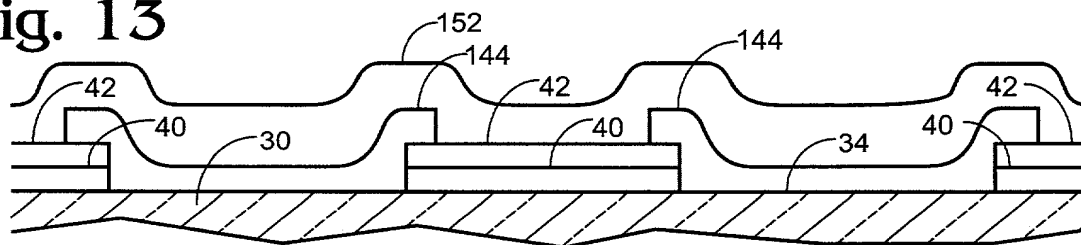


Fig. 13



10

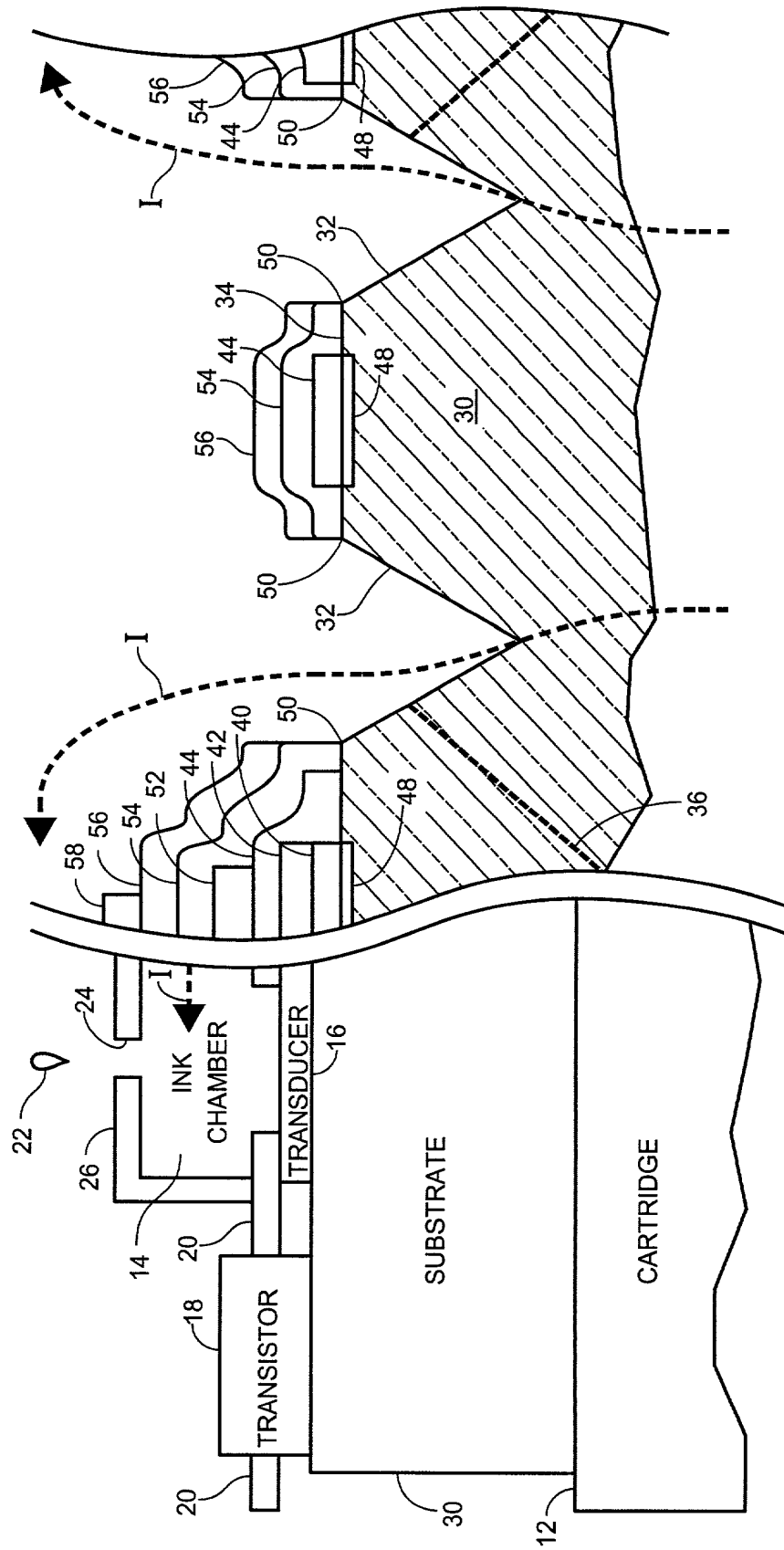


Fig. 14

Fig. 14 is a cross-sectional view of a semiconductor device. It shows a substrate with a patterned layer 40. On top of layer 40 are three rectangular blocks 42. Between the blocks are two curved regions 144. A layer 34 is located beneath the middle block 42. A dashed line 146 indicates a boundary or interface.

This cross-sectional view shows a substrate with a wavy, uneven surface. A thin layer, labeled 144, is deposited over the substrate. On top of this layer, there are several rectangular blocks or pillars, labeled 40. These pillars are separated by gaps or recesses, labeled 146. The top surface of the pillars is labeled 42. The side walls of the pillars are labeled 154. The gaps between the pillars are also labeled 144.

This cross-sectional view shows a central gate structure 146 on a substrate 34. The gate structure 146 is composed of a gate stack 40 and a gate cap 150. The gate stack 40 is flanked by side spacers 154 and a gate sidewall 150. The substrate 34 is shown with a dashed line indicating an underlying layer.

This cross-sectional view shows a central gate structure 40 on a substrate 132. The gate structure 40 is flanked by side regions 150. The substrate 132 is shown with a dashed line indicating a boundary. The top surface of the gate structure 40 is labeled 146. The side regions 150 are shown with a dashed line indicating a boundary. The top surface of the side regions 150 is labeled 154.

Fig. 19

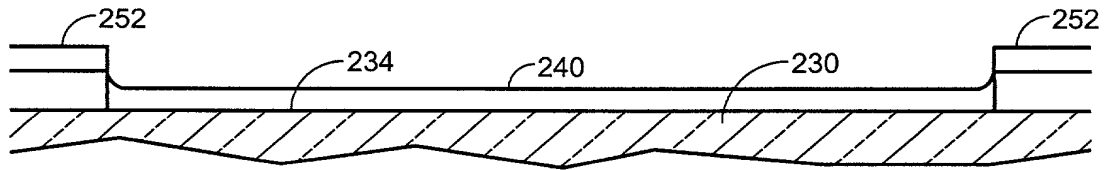


Fig. 20

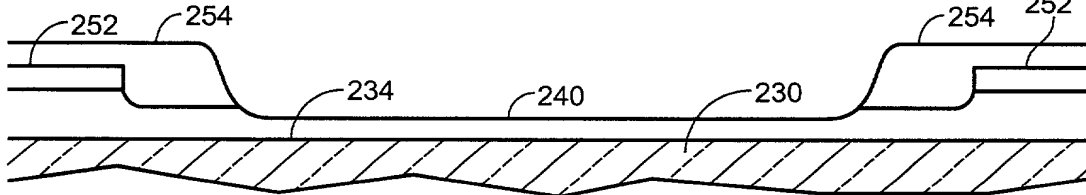


Fig. 21

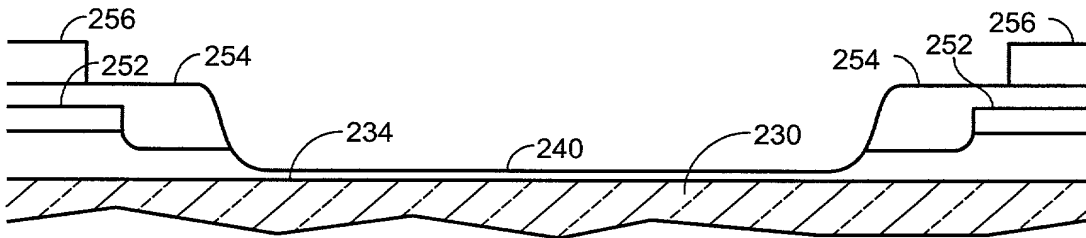


Fig. 22

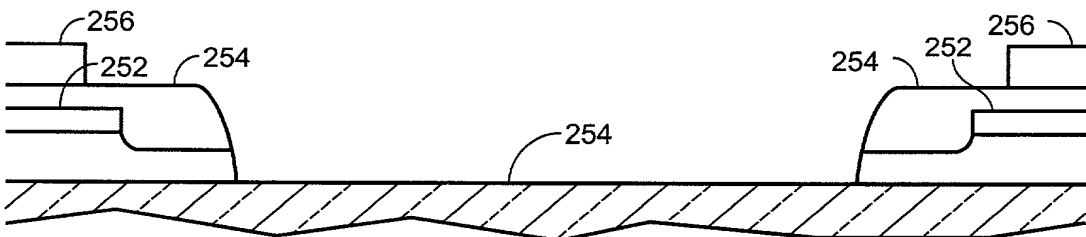


Fig. 23

